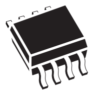
M41T56

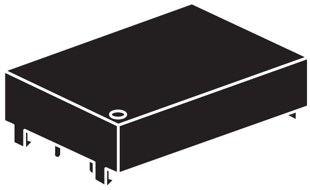
Serial Real Time Clock with 56 bytes NVRAM

Feature summary

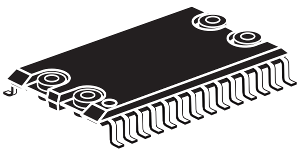
- Counters for seconds, minutes, hours, day, date, month, years, and century
- 32 KHz crystal oscillator integrating load capacitance (12.5pF) providing exceptional oscillator stability and high crystal series resistance operation
- Serial interface supports I^2C Bus (400kHz protocol)
- Ultra-low battery supply current of 450nA (typ@3V)
- 5V ±10% supply voltage
- Timekeeping down to 2.5V
- Automatic power-fail detect and switch circuitry
- 56 bytes of general purpose RAM
- Software clock calibration to compensate crystal deviation due to temperature
- Automatic leap year compensation
- Operating temperature of –40 to 85°C
- Packaging options include:
  - 28-lead SOIC and SNAPHAT® TOP (to be ordered separately)
  - SO8N

8

1

SO8N (M) 150mil width



SNAPHAT (SH) battery & crystal

28

1

SOH28 (MH)

Contents

List of tables

List of figures

1 Summary description

The M41T56 is a low power, Serial Real Time Clock with 56 bytes of NVRAM. A built-in 32,768Hz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two-line, bi-directional bus. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium coin cell.

Typical data retention time is in excess of 10 years with a 50mAh, 3V lithium cell. The M41T56 is supplied in an 8-lead Plastic SOIC package or a 28-lead SNAPHAT® package.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion. The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form.

For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4Txx-BR12SH” (see *Table 16 on page 26*).

Caution: Do not place the SNAPHAT battery/crystal package “M4Txx-BR12SH” in conductive foam as this will drain the lithium button-cell battery.

Figure 1. Logic diagram

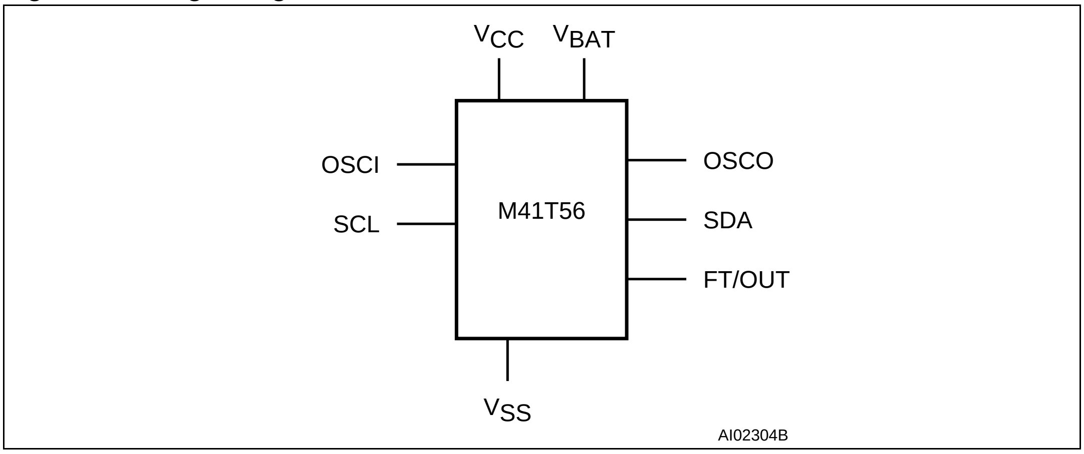


Table 1. Signal names

OSCI	Oscillator Input
OCSO	Oscillator Output
FT/OUT	Frequency Test / Output Driver (Open Drain)
SDA	Serial Data Address Input / Output
SCL	Serial Clock
V_{BAT}	Battery Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. 8-pin SOIC connections

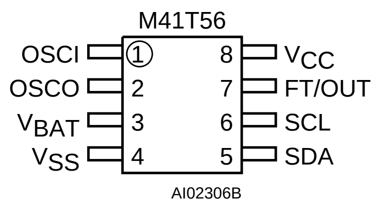


Figure 3. 28-pin SOIC connections

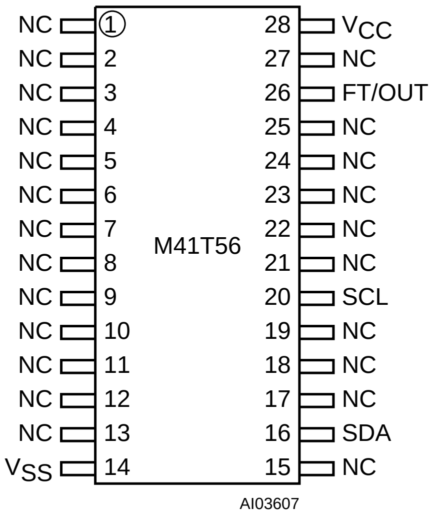
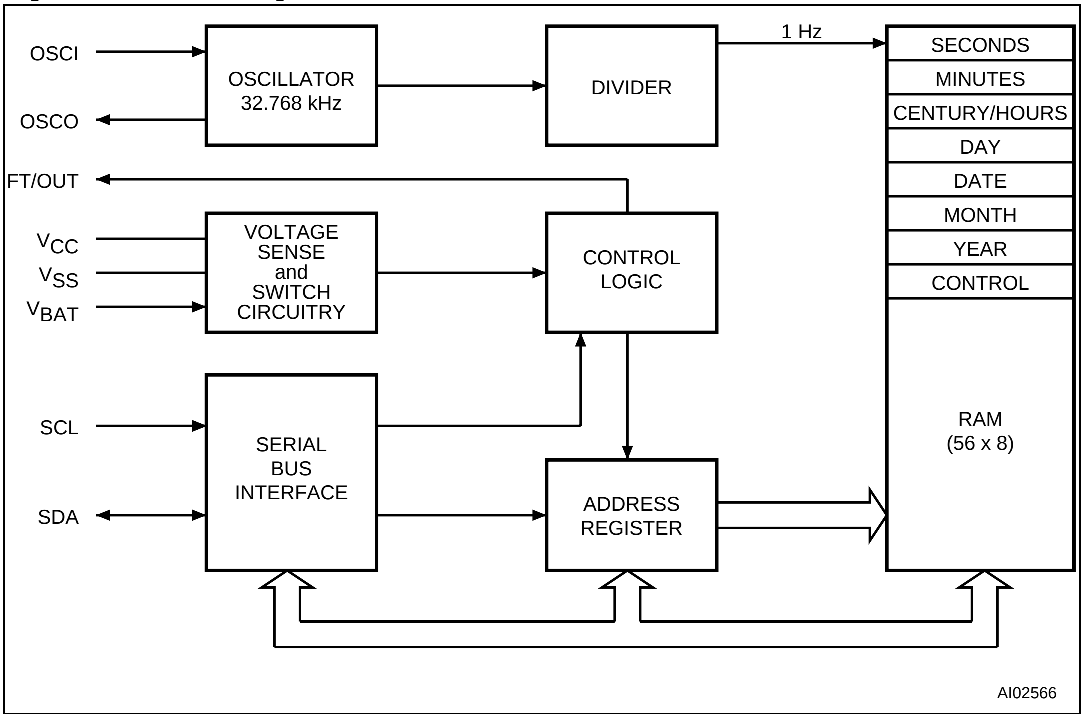


Figure 4. Block diagram



2 Operation

The M41T56 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds register
2. Minutes register
3. Century/hours register
4. Day register
5. Date register
6. Month register
7. Years register
8. Control register
9. RAM

The clock continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power-up, the device switches from battery to V_{CC} at V_{BAT} and recognizes inputs when V_{CC} goes above V_{PFD} volts.

2.1 2-wire bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High.
- Changes in the data line while the clock line is High will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain High.

2.1.2 Start data transfer

A change in the state of the data line, from High to Low, while the clock is High, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition, a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

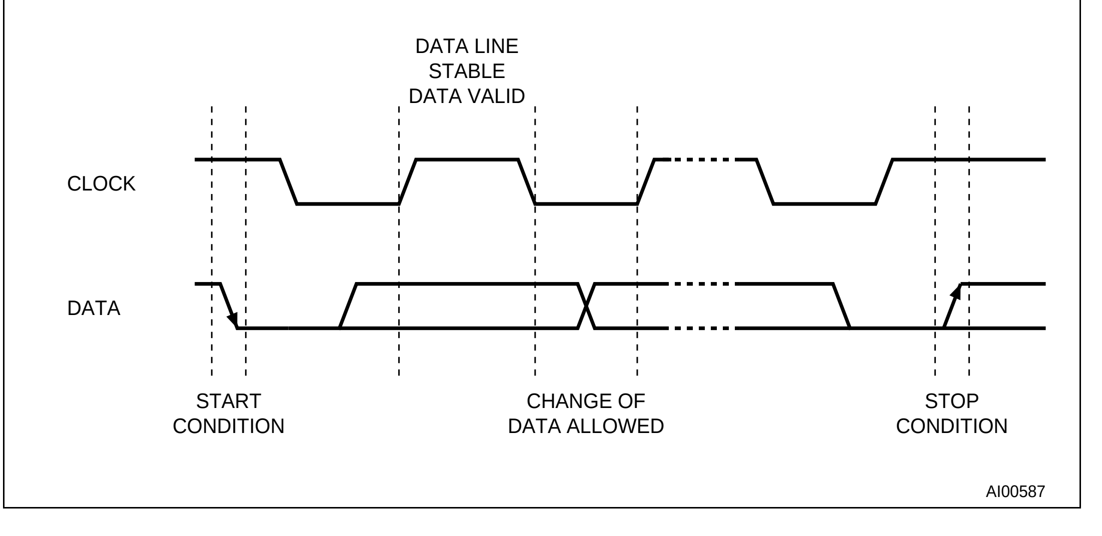


Figure 6. Acknowledge sequence

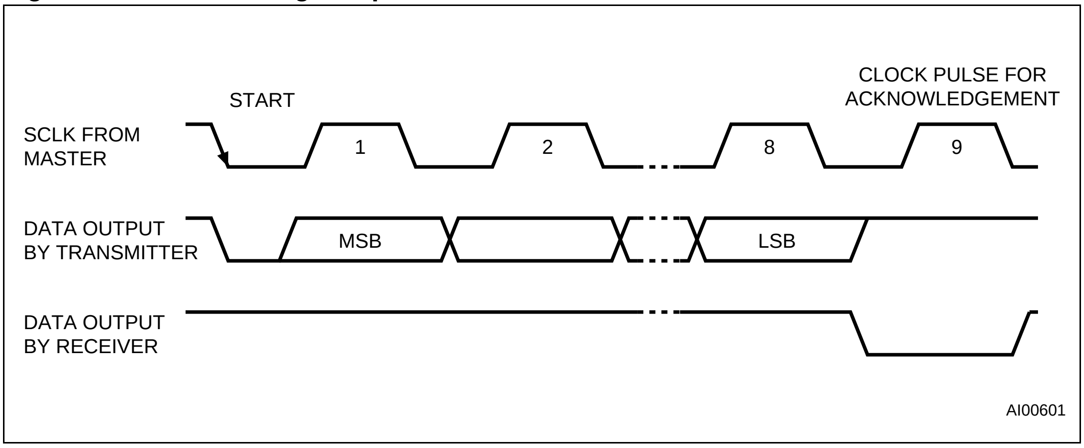


Figure 7. Bus timing requirements sequence

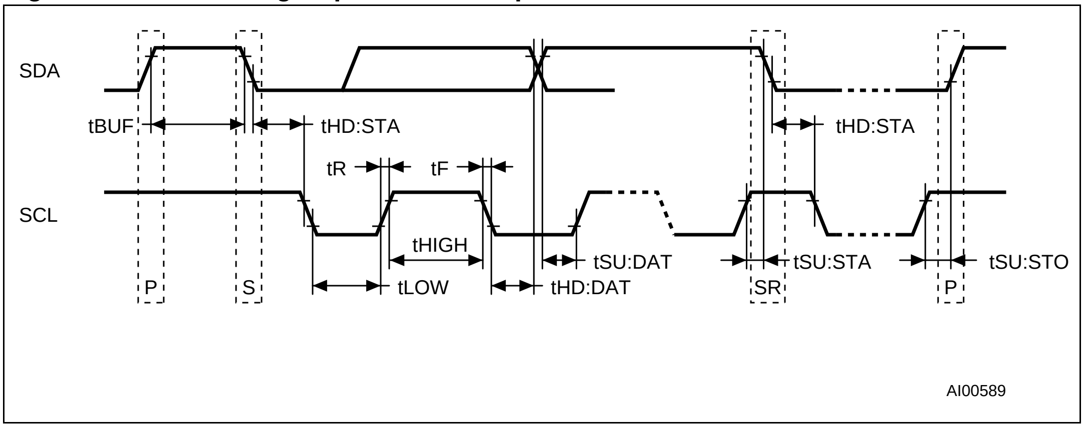


Table 2. AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
t_{LOW}	Clock low period	4.7		µs
t_{HIGH}	Clock high period	4		µs
t_R	SDA and SCL rise time		1	µs
t_F	SDA and SCL fall time		300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	4		µs
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	4.7		µs
$t_{SU:DAT}$	Data setup time	250		ns
$t_{HD:DAT}$[2]	Data hold time	0		µs
$t_{SU:STO}$	STOP condition setup time	4.7		µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs

1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

2.2 READ mode

In this mode, the master reads the M41T56 slave after setting the slave address (see *Figure 8 on page 12* and *Figure 9 on page 12*). Following the WRITE Mode Control Bit ($R/\overline{W}$ = 0) and the Acknowledge Bit, the word address A_n is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ Mode Control Bit ($R/\overline{W}$ = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an Acknowledge Bit to the slave transmitter. The address pointer is only incremented on reception of an Acknowledge Bit. The M41T56 slave transmitter will now place the data byte at address A_n + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to A_n + 2. This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented, whereby the master reads the M41T56 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer, see *Figure 10 on page 12*.

Figure 8. Slave address location

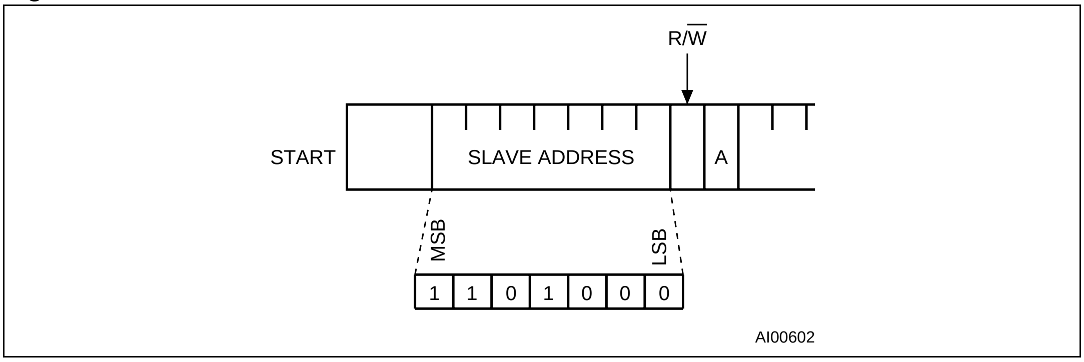


Figure 9. READ mode sequence

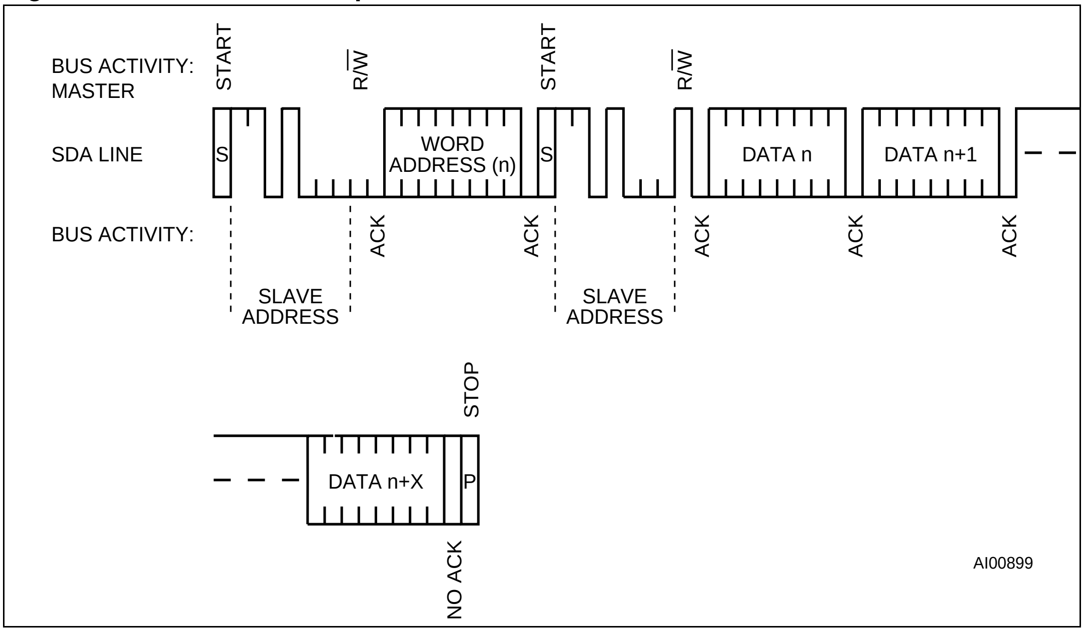
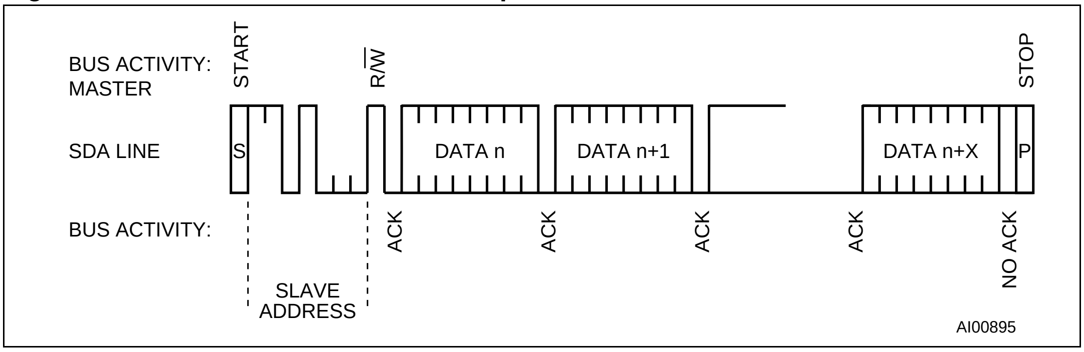


Figure 10. Alternative READ mode sequence



2.3 WRITE mode

In this mode the master transmitter transmits to the M41T56 slave receiver. Bus protocol is shown in *Figure 11 on page 13*. Following the START condition and slave address, a logic '0' ($R/\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address A_n will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41T56 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte (see *Figure 8 on page 12*).

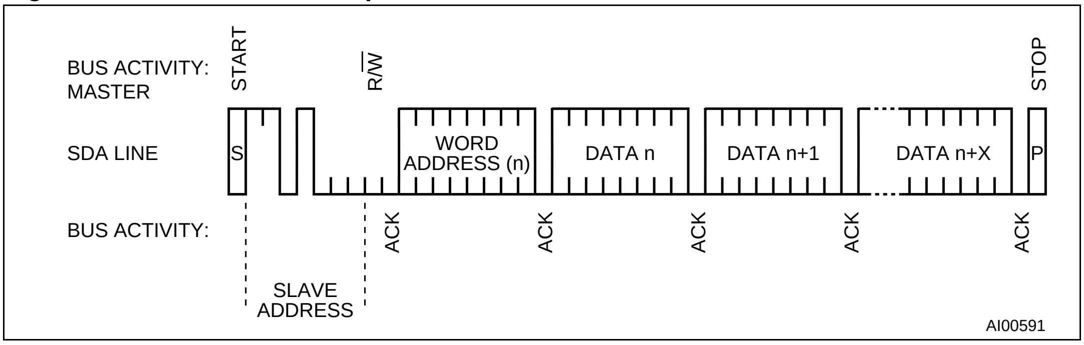
2.4 Data retention mode

With valid V_{CC} applied, the M41T56 can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41T56 will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min). This is accomplished by internally inhibiting access to the clock registers and SRAM. When V_{CC} falls below the Battery Back-up Switchover Voltage (V_{SO}), power input is switched from the V_{CC} pin to the battery and the clock registers and SRAM are maintained from the attached battery supply.

All outputs become high impedance. On power up, when V_{CC} returns to a nominal value, write protection continues for t_{REC}.

For a further more detailed review of battery lifetime calculations, please see Application Note AN1012.

Figure 11. WRITE mode sequence



3 Clock operation

The eight byte clock register (see *Table 3*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Seconds, Minutes, and Hours are contained within the first three registers. Bits D6 and D7 of Clock Register 2 (Hours Register) contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of Register 3 contain the Day (day of week). Registers 4, 5, and 6 contain the Date (day of month), Month, and Years. The final register is the Control Register (this is described in the Clock Calibration section). Bit D7 of Register 0 contains the STOP Bit (ST). Setting this bit to a '1' will cause the oscillator to stop.

If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The seven Clock Registers may be read one byte at a time, or in a sequential block. The Control Register (Address location 7) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250ms to allow the READ to be completed before the update occurs. This will prevent a transition of data during the READ.

Note: This 250ms delay affects only the clock register update and does not alter the actual clock time.

Table 3. Register map[1]

Address	Data								Function/range BCD format	
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	ST	10 Seconds			Seconds				Seconds	00-59
1	X	10 Minutes			Minutes				Minutes	00-59
2	CEB[2]	CB	10 hours		Hours				Century/hours	0-1/00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 date		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 years				Years				Year	00-99
7	OUT	FT	S	Calibration					Control	

1. Keys:
   S = SIGN Bit
   FT = FREQUENCY TEST Bit
   ST = STOP Bit
   OUT = Output level
   X = Don't care
   CEB = Century Enable Bit
   CB = Century Bit
2. When CEB is set to '1,' CB toggles from '0' to '1' or from '1' to '0' every 100 years (dependent upon the initial value set). When CEB is set to '0,' CB does not toggle.

3.1 Clock calibration

The M41T56 is driven by a quartz-controlled oscillator with a nominal frequency of 32,768Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M41T56 improves to better than ±2 ppm at 25°C.

The oscillation rate of any crystal changes with temperature (see *Figure 12 on page 16*). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The M41T56 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 12 on page 16*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five-bit Calibration Byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration Byte occupies the five lower order bits (D4-D0) in the Control Register (Addr 7). This byte can be set to represent any value between 0 and 31 in binary form. Bit D5 is the Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minutes cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768Hz, each of the 31 increments in the Calibration Byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41T56 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration Byte.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) Bit, the seventh-most significant bit in the Control Register, is set to a '1,' and the oscillator is running at 32,768Hz, the FT/OUT pin of the device will toggle at 512Hz. Any deviation from 512Hz indicates the degree and direction of oscillator frequency shift at the test temperature.

For example, a reading of 512.01024Hz would indicate a +20ppm oscillator frequency error, requiring a –10(XX001010) to be loaded into the Calibration Byte for correction.

Note: Setting or changing the Calibration Byte does not affect the Frequency Test output frequency.

Figure 12. Crystal accuracy across temperature

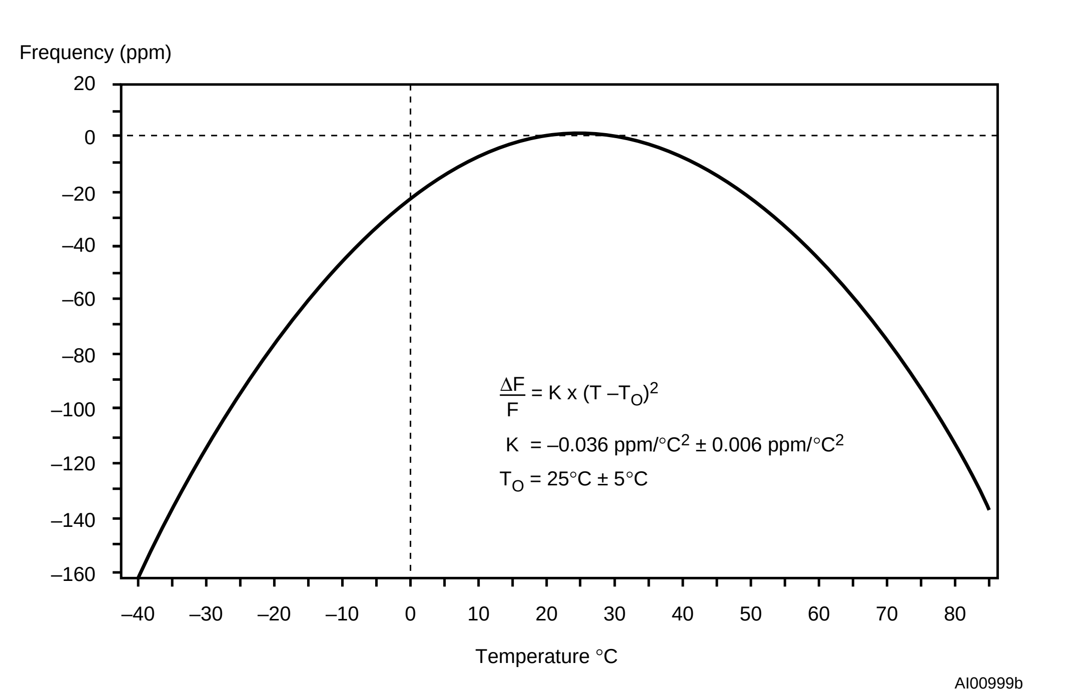
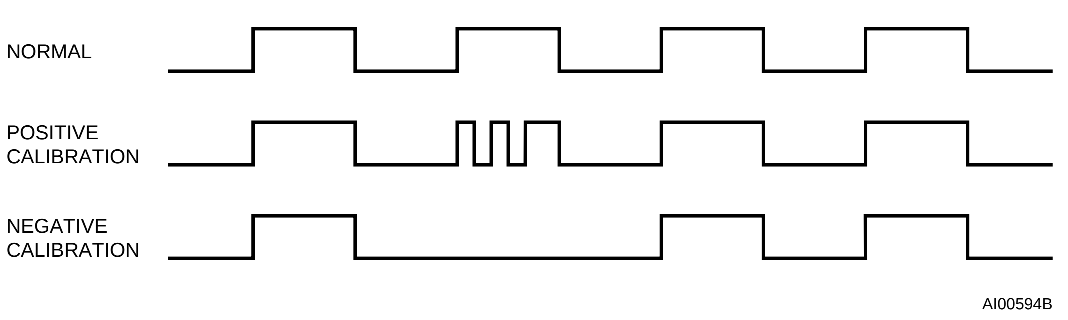


Figure 13. Clock calibration



3.2 Output driver pin

When the FT Bit is not set, the FT/OUT pin becomes an output driver that reflects the contents of D7 of the Control Register. In other words, when D6 of location 7 is a '0' and D7 of location 7 is a '0' and then the FT/OUT pin will be driven low.

Note: The FT/OUT pin is open drain which requires an external pull-up resistor.

3.3 Initial power-on defaults

Upon initial application of power to the device, the FT Bit will be set to a '0' and the OUT Bit will be set to a '1.' All other Register bits will initially power-on in a random state.

4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature		–40 to 85	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	SNAPHAT	–40 to 85	°C
		SOIC	–55 to 125	
T_{SLD}(1)(2)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.3 to 7	V
V_{CC}	Supply voltage		–0.3 to 7	V
I_O	Output current		20	mA
P_D	Power dissipation		0.25	W

1. For SO package, standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).
2. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 5. Operating and AC measurement conditions(1)

Parameter	Value	Unit
Supply Voltage (V_{CC})	4.5 to 5.5	V
Ambient Operating Temperature (T_A)	–40 to 85	°C
Load Capacitance (C_L)	100	pF
Input Rise and Fall Times	≤5	ns
Input Pulse Voltages	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	V

1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 14. AC measurement I/O Waveform

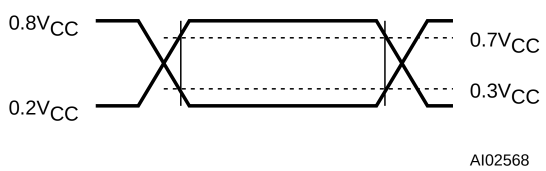


Table 6. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance (SCL)		7	pF
C_{OUT}(3)	Output capacitance (SDA, FT/OUT)		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)	0.25	1	µs

1. Effective capacitance measured with power supply at 5V; sampled, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 7. DC characteristics

Symbol	Parameter	Test condition(1)	Min	Typ	Max	Unit
I_{LI}	Input leakage current	$0V \leq V_{IN} \leq V_{CC}$			±1	µA
I_{LO}	Output leakage current	$0V \leq V_{OUT} \leq V_{CC}$			±1	µA
I_{CC1}	Supply current	Switch frequency = 100kHz			300	µA
I_{CC2}	Supply current (standby)	SCL, SDA = V_{CC} – 0.3V		100		µA
V_{IL}	Input low voltage		–0.3		1.5	V
V_{IH}	Input high voltage		3		V_{CC} + 0.8	V
V_{OL}	Output low voltage	I_{OL} = 5mA, V_{CC} = 4.5V			0.4	V
V_{BAT}(2)	Battery supply voltage		2.5	3	3.5	V
I_{BAT}	Battery supply current	T_A = 25°C, V_{CC} = 0V, oscillator ON, V_{BAT} = 3V		450	550	nA

1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5V (except where noted).
2. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.

Table 8. Crystal Electrical Characteristics

Symbol	Parameter(1)(2)(3)	Min	Typ	Max	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			60	kΩ
C_L	Load capacitance		12.5		pF

1. These values are externally supplied if using the SO8N package. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at kouhou@kdsj.co.jp or http://www.kdsj.co.jp for further information on this crystal type.
2. Load capacitors are integrated within the M41T56. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. All SNAPHAT battery/crystal tops meet these specifications.

Figure 15. Power down/up mode AC Waveforms

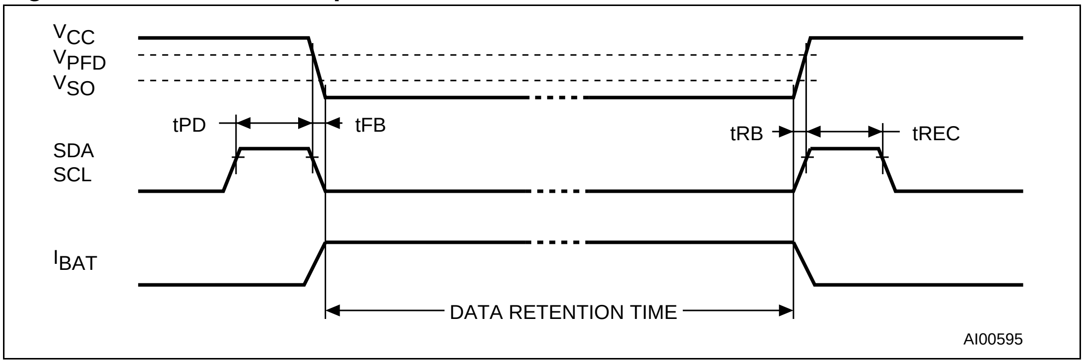


Table 9. Power down/up mode AC characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_{PD}	SCL and SDA at V_{IH} before power down	0		ns
t_{FB}	V_{PFD} (min) to V_{SS} V_{CC} fall time	300		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	100		µs
t_{REC}	SCL and SDA at V_{IH} after power up	10		µs

1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5V (except where noted).

Table 10. Power down/up trip points DC characteristics

Symbol	Parameter(1)(2)	Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	1.2 V_{BAT}	1.25 V_{BAT}	1.285 V_{BAT}	V
V_{SO}	Battery back-up switchover voltage		V_{BAT}		V

1. All voltages referenced to V_{SS}.
2. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5V (except where noted).

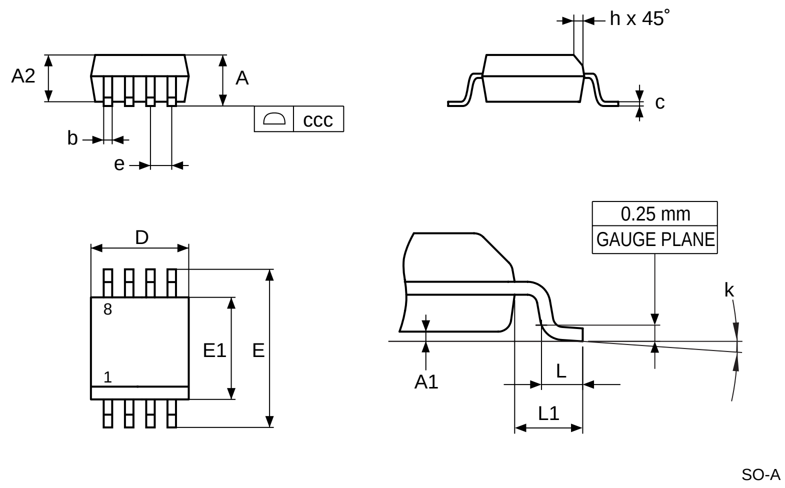
6 Package mechanical information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 16. SO8N – 8-pin plastic small package outline

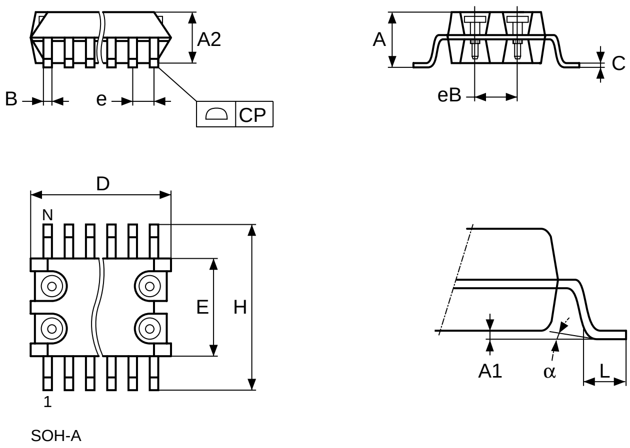


1. Drawing is not to scale.

Table 11. SO8N – 8-pin plastic small outline, package mechanical data

Symbol	millimetres			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 17. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT, package outline

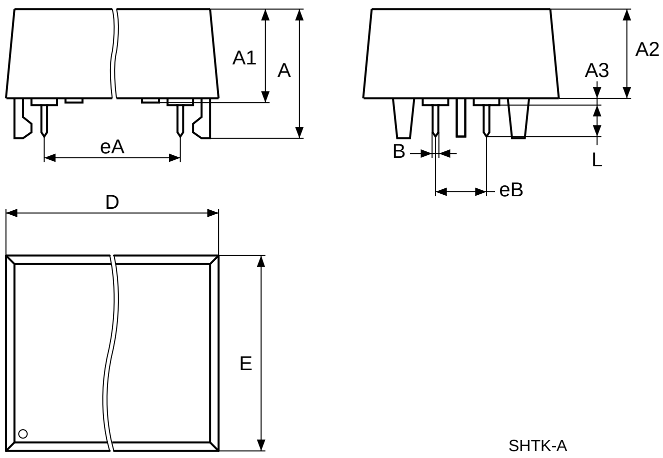


1. Drawing is not to scale.

Table 12. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT, mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 18. SH – 4-pin SNAPHAT housing for 48mAh battery & crystal, package outline

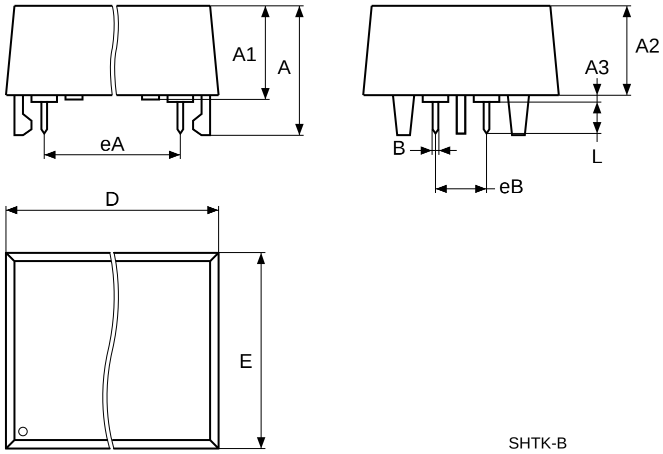


1. Drawing is not to scale.

Table 13. SH – 4-pin SNAPHAT housing for 48mAh battery & crystal, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		.6122	.6280
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 19. SH – 4-pin SNAPHAT housing for 120mAh battery & crystal, package outline



1. Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT housing for 120mAh battery & crystal, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		.6122	.6280
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

7 Part numbering

Table 15. Ordering information scheme

Example:	M41T	56	M	6	E

Device type

M41T

Supply voltage and write protect voltage

56 = V_{CC} = 4.5 to 5.5V

Package

M = SO8N

MH(1)= SOH28

Temperature range

6 = –40 to 85°C

Shipping method

For SO8N:

E = Lead-free package (ECOPACK®), tubes

F = Lead-free package (ECOPACK®), tape & reel

For SOH28:

E = Lead-free package (ECOPACK®), tubes

F = Lead-free Package (ECOPACK®), tape & reel

1. The SOIC package (SOH28) requires the SNAPHAT® battery package which is ordered separately under the part number “M4Txx-BR12SHx” in plastic tube or “M4Txx-BR12SHxTR” in Tape & Reel form (see *Table 16*).

Caution: Do not place the SNAPHAT battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

Table 16. SNAPHAT battery/crystal table

Part number	Description	Package
M4T28-BR12SH	Lithium battery (48mAh)/crystal SNAPHAT	SH
M4T32-BR12SH	Lithium battery (120mAh)/crystal SNAPHAT	SH

8 Revision history

Table 17. Document revision history

Date	Rev. #	Revision details
March 1999	1.0	First issue
12/23/99	1.1	SOH28 package added
03/21/00	1.2	Series resistance Max Value changed (*Table 8*)
11/30/00	1.3	Added PSDIP8 package
01/25/01	1.4	Corrected graphic, measurements of PSDIP8 (Figure 18, Table 14)
02/16/01	2.0	Reformatted, table added (*Table 16*)
04/06/01	2.1	Add temp./voltage information to characteristics (*Table 7*, *Table 2*); correct Series Resistance (*Table 8*)
07/17/01	2.2	Basic formatting changes
08/02/02	2.3	Modify reflow time and temperature footnote (*Table 4*); modify Crystal Electrical Characteristics table footnotes (*Table 8*); removed PSDIP8 package
11/07/02	2.4	Correct figure name (*Feature summary on page 1*)
15-Jun-04	3.0	Reformatted; add Lead-free information; update characteristics (*Figure 12*; *Table 4*, *Table 15*)
11-Sep-2006	4	Changed document to new template; amalgamated diagrams in *Feature summary on page 1*; amended footnotes in *Table 3: Register map*; updated Package mechanical data in *Section 6: Package mechanical information*; small text changes for entire document, removed lead packages from *Table 15*, ECOPACK compliant
09-Oct-2006	5	Updated package mechanical data in *Figure 16.: SO8N – 8-pin plastic small package outline*.